# Simplified VHDL Coding of Modified Non-Restoring Square Root Calculator

## Abstract

Square root calculation is one of the most useful and vital operations in digital signal processing, the operation which in recent generations of processors is performed by the hardware. The hardware implementation of the square root operation can be achieved by different means, but it is very dependent on programmer's sense and ability to write efficient hardware designs. This paper offers universal and shortest VHDL coding of modified non-restoring square root calculator. The main principle of the method is similar with conventional non-restoring algorithm, but it only uses subtract operation and append 01, while add operation and append 11 is not used. The strategy has been conducted to implement it successfully in FPGA hardware, and offer an efficient in hardware resource, and it is superior.